B Instruction Summary

Load instructions			
Instruction	**Description**	**Operation**	**Bits of the SREG that are affected**
MOV Rd,Rs	Loading from register to register (8bit) d,s ϵ [0,31]	Rd=Rs	-
MOVW Rd,Rs	Loading from register to register (16bit) d,s ϵ {0,2,…,30}	Rd+1:Rd=Rs+1:Rs	-
LDI Rd,k	Loading an integer to a register (integer value) d ϵ [16,31], k ϵ [0,255]	Rd=k	-
LD Rd,X	Loading (indirect) from a memory location (pointed by X) to a register d ϵ [0,31]	Rd=(X)	-
LD Rd,X+	Loading (indirect) from a memory location (pointed by X) to a register and X increment by 1 (after) d ϵ [0,31]	Rd=(X) X=X+1	-
LD Rd,-X	X decrement by 1 (before) and Loading (indirect) from a memory location (pointed by X) to a register d ϵ [0,31]	X=X-1 Rd=(X)	-
LD Rd,Y	Loading (indirect) from a memory location (pointed by Y) to a register d ϵ [0,31]	Rd=(Y)	-
LD Rd,Y+	Loading (indirect) from a memory location (pointed by Y) to a register and Y increment by 1 (after) d ϵ [0,31]	Rd=(Y) Y=Y+1	-
LD Rd,-Y	Y decrement by 1 (before) and Loading (indirect) from a memory location (pointed by Y) to a register d ϵ [0,31]	Y=Y-1 Rd=(Y)	-
LDD Rd,Y+q	Loading (indirect) from a memory location (pointed by Y+q) to a register (q is an integer value) d ϵ [0,31]	Rd=(Y+q)	-
LD Rd,Z	Loading (indirect)	Rd=(Z)	-

	from a memory location (pointed by Z) to a register d ϵ [0,31]		
LD Rd,Z+	Loading (indirect) from a memory location (pointed by Z) to a register and Z increment by 1 (after) d ϵ [0,31]	Rd=(Z) Z=Z+1	-
LD Rd,-Z	Z decrement by 1 (before) and Loading (indirect) from a memory location (pointed by Z) to a register d ϵ [0,31]	Z=Z-1 Rd=(Z)	-
LDD Rd,Z+q	Loading (indirect) from a memory location (pointed by Z+q) to a register (q is an integer value) d ϵ [0,31]	Rd=(Z+q)	-
LDS Rd,addr	Loading (direct) a register from a memory location (RAM) d ϵ [0,31]	Rd=(addr)	-
ST X,Rs	Loading (indirect) from a register to a memory location (pointed by X) s ϵ [0,31]	(X)=Rs	-
ST X+,Rs	Loading (indirect) from a register to a memory location (pointed by X) and X increment by 1 (after) s ϵ [0,31]	(X)=Rs X=X+1	-
ST –X,Rs	X decrement by 1 (before) and Loading (indirect) a register to a memory location (pointed by X) s ϵ [0,31]	X=X-1 (X)=Rs	-
ST Y,Rs	Loading (indirect) from a register to a memory location (pointed by Y) s ϵ [0,31]	(Y)=Rs	-
ST Y+,Rs	Loading (indirect) from a register to a memory location (pointed by Y) and Y increment by 1 (after) s ϵ [0,31]	(Y)=Rs Y=Y+1	-
ST –Y,Rs	Y decrement by 1 (before) and Loading (indirect) a register to a memory location (pointed by Y) s ϵ [0,31]	Y=Y-1 (Y)=Rs	-
STD Y+q,Rs	Loading (indirect) from a register to a memory location (pointed by Y+q), q is an integer value s ϵ [0,31]	(Y+q)=Rs	-
ST Z,Rs	Loading (indirect) from a register to a memory location (pointed by Z) s ϵ [0,31]	(Z)=Rs	-
ST Z+,Rs	Loading (indirect)	(Z)=Rs	-

	from a register to a memory location (pointed by Z) and Z increment by 1 (after) s ϵ [0,31]	Z=Z+1	
ST –Z,Rs	Z decrement by 1 (before) and Loading (indirect) a register to a memory location (pointed by Z) s ϵ [0,31]	Z=Z-1 (Z)=Rs	-
STD Z+q,Rs	Loading (indirect) from a register to a memory location (pointed by Z+q), q is an integer value s ϵ [0,31]	(Y+q)=Rs	-
STS addr,Rs	Loading (direct) a memory location (RAM) from a register s ϵ [0,31]	(addr)=Rs	-

Arithmetic and Logical instructions

Instruction	Description	Operation	Bits of the SREG that are affected
ADD Rd,Rs	Add two registers (without carry) d,s ϵ [0,31]	Rd=Rd+Rs	H,S,V,N,Z,C
ADC Rd,Rs	Add two registers with carry d,s ϵ [0,31]	Rd=Rd+Rs+C	H,S,V,N,Z,C
ADIW Rd,k	Add an integer value to a 16bit registers pair d ϵ {24,26,28,30}, k ϵ [0,63]	Rd+1:Rd=Rd+1:Rd+k	S,V,N,Z,C
SUB Rd,Rs	Subtract two registers (without carry) d,s ϵ [0,31]	Rd=Rd-Rs	H,S,V,N,Z,C
SUBI Rd,k	Subtract an integer value from a register d ϵ [16,31], k ϵ [0,255]	Rd=Rd-k	H,S,V,N,Z,C
SBC Rd,Rs	Subtract two registers with carry d,s ϵ [0,31]	Rd=Rd+Rs-C	H,S,V,N,Z,C
SBCI Rd,k	Subtract an integer value and the carry from a register d ϵ [16,31], k ϵ [0,255]	Rd=Rd-k-C	H,S,V,N,Z,C
SBIW Rd,k	Subtract an integer value from a 16bit registers pair d ϵ {24,26,28,30}, k ϵ [0,63]	Rd+1:Rd=Rd+1:Rd-k	S,V,N,Z,C
AND Rd,Rs	Logical AND between two registers d,s ϵ [0,31]	Rd=Rd AND Rs	S,V=0,N,Z
ANDI Rd,k	Logical AND between a register and an integer value d ϵ [16,31], k ϵ [0,255]	Rd=Rd AND k	S,V=0,N,Z
OR Rd,Rs	Logical OR between registers d,s ϵ [0,31]	Rd=Rd OR Rs	S,V=0,N,Z
ORI Rd,k	Logical OR between a register and an integer value d ϵ [16,31], k ϵ [0,255]	Rd=Rd OR k	S,V=0,N,Z

EOR Rd,Rs	Logical EXCLUSIVE OR between two registers d,s ϵ [0,31]	Rd=Rd XOR Rs	S,V=0,N,Z
COM Rd	Logical NOT (one's complement) of a register content d ϵ [0,31]	Rd=0xFF-Rd	S,V=0,N,Z,C=1
NEG Rd	Two's complement calculation of a register content d ϵ [0,31]	Rd=0x00-Rd	H,S,V,N,Z,C
INC Rd	Increment the register content by 1 d ϵ [0,31]	Rd=Rd+1	S,V,N,Z
DEC Rd	Decrement the register content by 1 d ϵ [0,31]	Rd=Rd-1	S,V,N,Z
CLR Rd	Clear the register content d ϵ [0,31]	Rd=0x00	S=0,V=0,N=0,Z=1
SER	Load the maximum value on a register d ϵ [16,31]	Rd=0xFF	-
MUL Rd,Rs	Unsigned numbers multiplication through registers d,s ϵ [0,31]	R1:R0=Rd*Rs	Z,C
MULS Rd,Rs	Signed numbers multiplication through registers d,s ϵ [16,31]	R1:R0=Rd*Rs	Z,C
MULSU Rd,Rs	Signed/Unsigned numbers multiplication trhough registers d,s ϵ [16,23]	R1:R0=Rd*Rs	Z,C
FMUL	Unsigned fractioned numbers multiplication d,s ϵ [16,23]	R1:R0=Rd*Rs	Z,C
FMULS	Signed fractioned numbers multiplication d,s ϵ [16,23]	R1:R0=Rd*Rs	Z,C
FMULSU	Multiplication of a signed fractioned number with an unsigned fractioned number d,s ϵ [16,23]	R1:R0=Rd*Rs	Z,C

Shift and bit manipulation instructions

Instruction	Description	Operation	Bits of the SREG that are affected
LSL Rd	Logical shift left d ϵ [0,31]	C=Rd(7) Rd(n+1)=Rd(n) Rd(0)=0	Z, C, N, V, H
LSR Rd	Logical shift right d ϵ [0,31]	C=Rd(0) Rd(n)=Rd(n+1) Rd(7)=0	Z, C, N, V
ROL Rd	Shift left through carry d ϵ [0,31]	Rd(0)=C Rd(n+1)=Rd(n) C=Rd(7)	Z, C, N, V, H

ROR Rd	Shift right through carry d ϵ [0,31]	Rd(7)=C Rd(n)=Rd(n+1) C=Rd(0)	Z, C, N, V
ASR Rd	Arithmetical shift right through carry d ϵ [0,31]	Rd(n)=Rd(n+1), n=0..6	Z, C, N, V
SWAP Rd	Swap High/Low Parts of a register d ϵ [0,31]	Rd(3..0)⇔Rd(7..4)	-
BSET s	Sets a specific bit in the SREG s ϵ [0,7]	SREG(s) = 1	SREG(s)
BCLR s	Clears a specific bit in the SREG s ϵ [0,7]	SREG(s) = 0	SREG(s)
SEC	Sets the bit C of SREG	C=1	C
CLC	Clears the bit C of SREG	C=0	C
SEN	Sets the bit N of SREG	N=1	N
CLN	Clears the bit N of SREG	N=0	N
SEZ	Sets the bit Z of SREG	Z=1	Z
CLZ	Clears the bit Z of SREG	Z=0	Z
SEI	Sets the bit I of SREG	I=1	I
CLI	Clears the bit I of SREG	I=0	I
SES	Sets the bit S of SREG	S=1	S
CLS	Clears the bit S of SREG	S=0	S
SEV	Sets the bit V of SREG	V=1	V
CLV	Clears the bit V of SREG	V=0	V
SET	Sets the bit T of SREG	T=1	T
CLT	Clears the bit T of SREG	T=0	T
SEH	Sets the bit H of SREG	H=1	H
CLH	Clears the bit H of SREG	H=0	H